

What's with capacitance, dielectrics on a PCB?

Steve Huang
March 9, 2006

A co-worker of mine recently sent me an e-mail from an experienced engineer he met during the EMC Technology meeting, discussing some electrical principles and fundamentals. In a snippet, the e-mail read, "Since c [capacitance] is higher on an outer layer, a given physical length is electrically shorter (smaller number of wavelengths)." Knowing the answer full well, my co-worker doubled checked with the person only to confirm he fully believed his argument was correct. Let's examine this statement.

While not always true, in general, the capacitance C on the outer layer of a printed circuit board (PCB) is lower than the capacitance on the inner layers. Why is that?

The simplest way to think about capacitance is to relate it back to the formula for a parallel plate capacitor, which is:

$$C = \frac{\epsilon A}{d} \text{ (eqn 1)}$$

where A is the area of the plate, ϵ is the relative dielectric constant, and d is the distance between the two plates. The parameters we can change are A, epsilon, and spacing.

Let's do a simple calculation. Using equation (1), let deduce the capacitance of a 10x10mil parallel plate. Suppose the ground and trace are both 10 mils wide, the space is 10 mils, and the dielectric is 4.0. In a 10x10 mil area, substituting the numbers, we find the capacitance is 1 mF.

Although the result seems small, in a PCB the geometry the capacitance is even smaller! A larger ground plane contributes to a different geometry, which significantly lowers the capacitance between ground and trace. On average, the capacitance is 10⁶ times smaller! Depending on the geometry, dielectric material, and lossy parameters, the capacitance ranges from a few pFs to several hundred pFs.

The same intuition from equation 1 still applies to the trace to ground capacitance C_{t_g} of a PCB - as trace area increases, C_{t_g} increases; as spacing decreases between the trace and plane, C_{t_g} increases; and as ϵ increases, C_{t_g} increases proportionally.

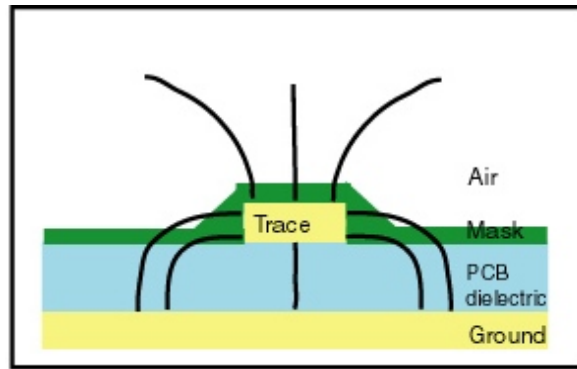


Figure 1. In a microstrip configuration the electric field lines penetrate both air and pcb dielectric.

In the case of a microstrip layout, the electric fields penetrate both the space above and below the trace (see Figure 1). Below the trace, the dielectric constant is composed of the PCB dielectric, typically around 4.0 for standard FR-4 materials. Above the trace the electric field penetrates the solder mask and air, which has an overall lower dielectric constant than that of the PCB material, e.g. solder mask has $\epsilon = 3.1$ and air has $\epsilon = 1$. Because electric field lines pass through a heterogeneous mix of the PCB material, solder mask, and air, the total dielectric constant is lower than a trace surrounded by PCB material, i.e. stripline configuration.

Since the total dielectric constant is lower in a microstrip than a stripline, from our intuition, we can say the C_{t_g} is lower in a microstrip configuration than a stripline configuration.

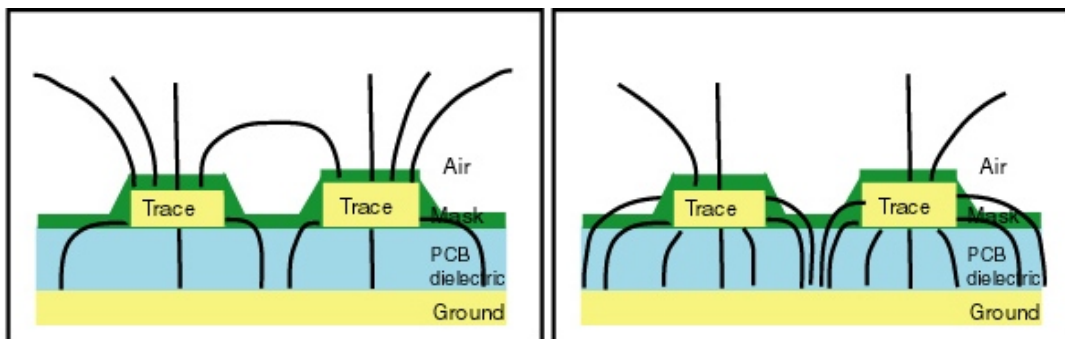


Figure 2. In a differential coupled signal (left) more electric field lines are in the air for odd-mode, while (right) more electric field lines are in the dielectric for even-mode.

There are some other interesting tidbits to know. In differential coupled traces, there are more electric field lines in the air when viewing the odd mode signal as compared to the electric field lines in even mode. In even mode, there are more electric field lines in the PCB. Still the total effective dielectric constant in a microstrip differential coupled configuration is less than that of a stripline differential coupled configuration.

Because the odd and even mode electric fields differ, the total effective dielectric differs between the two modes as well. The odd mode total effective dielectric ϵ_{ODD} is less than

the even mode total effective dielectric ϵ_{EVEN} . Using a well known equation describing the signal velocity within a dielectric, where c is the constant of speed of light,

$$v_p = \frac{c}{\sqrt{\epsilon}} \text{ (eqn 2),}$$

we can deduce, $v_{p(\text{even})}$ is less than $v_{p(\text{odd})}$ in a microstrip configuration. So the propagation velocity is higher in odd mode than in even mode. This means there is more jitter in a differential microstrip configuration when compared to a differential stripline. However the signal will travel faster, up to twice the speed depending on the PCB materials used.

Let's briefly discuss the conclusion of the statement introduced before, "a given physical length is electrically shorter (smaller number of wavelengths)." Electrical length, in this case, refers the time it take to travel in a certain times, i.e. propagation delay. To calculate the electric length, we apply the formula

$$\text{Electrical length} = d[m] / v_p [m/s] \text{ (eqn 3),}$$

where $v_p [m/s]$ is velocity of the signal (from eqn 2) and d is the distance.

So, if the capacitance is lower on the outer trace (microstrip) because the velocity is increased when compared to a stripline and thus for a given physical length the electrical length is shorter indeed. The answer was correct, but the intuition was wrong.